Q.P. Code: 16EC408 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations February-2022

COMPUTER ORGANIZATION AND ARCHITECTURE

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Explain the phases involved in Instruction cycle with the help of necessary timing diagrams?	**7M**
	b	Write about hierarchy of buses, bus signals and its functionalities.	**5M**
		OR	
2	**a**	Sketch the internal organization of CPU out with its functionalities and block diagram.	**6M**
	b	Elaborate how CPU is concordant with its Input & Output devices and explain the interfacing modules involved?	**6M**
		UNIT-II	
3	**a**	Elaborate the steps involved in execution of Memory-Reference instructions with its timing signals.	**6M**
	b	Explain the Memory-Reference instructions with examples.	**6M**
		OR	
4	**a**	Tabulate the Input-Output Instructions using register transfer notations?	**6M**
	b	Illustrate the phases of Interrupt Cycle with a neat flowchart	**6M**
		UNIT-III	
5	**a**	Explain the logical micro operations which manipulates individual bits of word in register with examples.	**6M**
	b	Implement a 4-bit combinational circuit shifter using Multiplexer.	**6M**
		OR	
6	**a**	Demonstrate the general configuration of Micro programmed Control unit with a neat block diagram.	**4M**
	b	Explain about address sequencing in control memory with neat diagrams?	**8M**
		UNIT-IV	
7	**a**	Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost?	**8M**
	b	Write about Auxiliary memory devices.	**4M**
		OR	
8	**a**	Brief out the hardware organization of Associative memory with diagrams.	**6M**
	b	What is Locality of Reference and explain about Cache memory in detail.	**6M**
		UNIT-V	
9	**a**	Justify how parallel processing improves the performance of multiprocessing environment?	**6M**
	b	Illustrate a processor with multiple functional units with a neat diagram.	**6M**
		OR	
10	**a**	Illustrate the behavior of a pipeline using space-time diagram.	**6M**
	b	A non-pipeline system takes 50ns to process a task. The same task can be processed in a six –segment pipeline with a clock of 10 ns. Determine speedup ratio of the pipeline for 100 tasks.	**6M**

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